Semiconductor Consortia in Japan: Experiences and Lessons

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Consortia for Device Technologies

MIRAI (2002/8)

; Millenium Research for Advanced Information Technology

Selete (2001/4～2006/3)

; Semiconductor Leading Edge Technologies, Inc.

ASPLA (2002/7)

; Advanced SoC Platform Corporation

STARC (1995/12)

; Semiconductor Technology Academic Research Center

Consortia for Equipment

HALCA (2001/8～2004/3)

; Highly Agile Line Concept Advancement

EUVA (2002/6～2006/3)

; Extreme Ultraviolet Lithography System Development Association

ASET (1996/2)

; Association of Super-Advanced Electronics Technologies

LEEPL (2000/6)

; Low Energy E-beam Proximity Projection Lithography

Consortia for Materials

SiP (2002/8)

; System in Package Consortium

CASMAT (2003/3)

; Consortium for Advanced Semiconductor Materials and Related Technologies

Others

VDEC ; VLSI Design Education Center

DIIN; New Intelligence for IC Differentiation

What happened in semiconductor industry(?256K)

	Business Matter	Technological Matter
16K	▪ **Japanese Companies' entry into the semiconductor industry** ▪ **R&D Consortium for VLSI**	▪ **Plasma equipment had come into wide use.** ▪ **Automatic controlled equipment became popular**
64K	▪ **3 Japanese makers entered into top 4 DRAM supplier**	▪ **New process technologies (RIE, Sputtering, Ion implantation, etc) appeared**
256K	▪ **Japanese DRAM occupied 80% of word 256k DRAM market** ▪ **Intel quitted DRAM business**	▪ **Stepper and Plasma CVD appeared** ▪ **Single-wafer equipment**

What happened in semiconductor industry (1M?)

1M	▪ **Korean Companies' entry into DRAM business**	▪ **Cluster tools appeared** ▪ **Chip companies gave up developing in-house equipment.** ▪ **Stacked capacitor and Trench capacitor appeared**
4M	▪ **Samsung became no. 1 DRAM supplier.**	▪ **I-line stepper** ▪ **Oligopolizing of equipment suppliers**
16M	▪ **NEC was only 1 Japanese company in top 4 DRAM suppliers.**	▪ **KrF stepper** ▪ **Popularizing of CMP**
64M	▪ **Rapid growth of Taiwanese companies in DRAM market.**	▪ **AMAT advocated "Total solution"** ▪ **Cu wiring and Low-k insulator were introduced into the LSI processing.**

Research Schedule

ASET Projects		R&D Targets	Money (-FY2007)	H7 95	H8 96	H9 97	H10 98	H11 99	H12 00	H13 01	H14 02	H15 03	H16 04	H17 05	H18 06	H19 07
Super Advanced Technology																
Semicon.	EB DW	High speed EB direct writing	32	←	—	—	→									
	EB Mask Writer	High accuracy EB mask writer	22	←	—	—	→									
	EB Lithography	Advanced EB technology	12				←	—	—	→						
	PXL	Proximity X ray Lithography	62	←	—	—	—	—	→							
	EUV	Extreme Ultraviolet Lithography	75				←	—	—	→						
	ArF Lithography	ArF lithography	17	←	—	→										
	Plasma	Plasma physics and diagnostics	25	←	—	—	—	—	→							
	Cleaning	Surface cleaning and simulation	8	←	—	—	—	—	→							
Mag Storage	Magnetic Storage	40Gbit/in2 class hard disk technology	57	←	—	—	—	—	→							
LCD	Reflective LCD	Reflective LCD material and devices	82	←	—	—	—	—	→							
EUV Absolute Wave Front		EUV absolute wave front measurement system	6							←	→					
EUV Process Technology		EUV mask and resisit process technology	11								←	—	4	—	→	
Equipment	Process equipment	Plasma equipment, Eximer laser	29					←	→							
	Simulation	FTP, Probe card	4						←	→						
	F2 Lithography	F2 light source, coating, purging	20						←	—	→					
PFC Substitution Process		Reduction of PFC in etching process, PFC free new wiring technology	62					←	—	—	—	→				
Electronic System Integration		3D packaging, Optical/electrical combined printed circuit boards	47					←	—	—	—	→				
Optical Packaging Standardization		Following Electronic System Integration Standardization of optical interconnection between boards and active interposers	1										1	→		
MIRAI Project		High-k gate stack, Low-k interconnect module, New transistor, etc	151							←	—	→	35	—	—	→
HALCA Project		Energy saving, miniline concept fab for SoCs	82							←	—	→				
High Efficiency Semiconductor Manufacturing Tool		Following HALCA Stencil mask, 300mm FTP, CMP	–										→	→	→	→
F.S. for Mask D2I		Feasibility Study of the Optimization Technology of Mask Design, Drawing, and Inspection for 45nm hp System LSI	–											↔		

ASET: Semiconductor Process Technology (First Stage)

ASET has various lithography technology development programs started in 1996. They are Electron Beam Direct Writing Technology, Electron Beam Mask Writing Technology, ArF Eximer Laser Lithography Technology and Proximity X-Ray Lithography Technology. Former 3 programs have been completed and some of the research results are used for commercial production.

ASET is also conducting Plasma Science and Diagnostics Technology and Surface Cleaning Technology necessary for very small pattering and fabrication of next generations of semiconductors

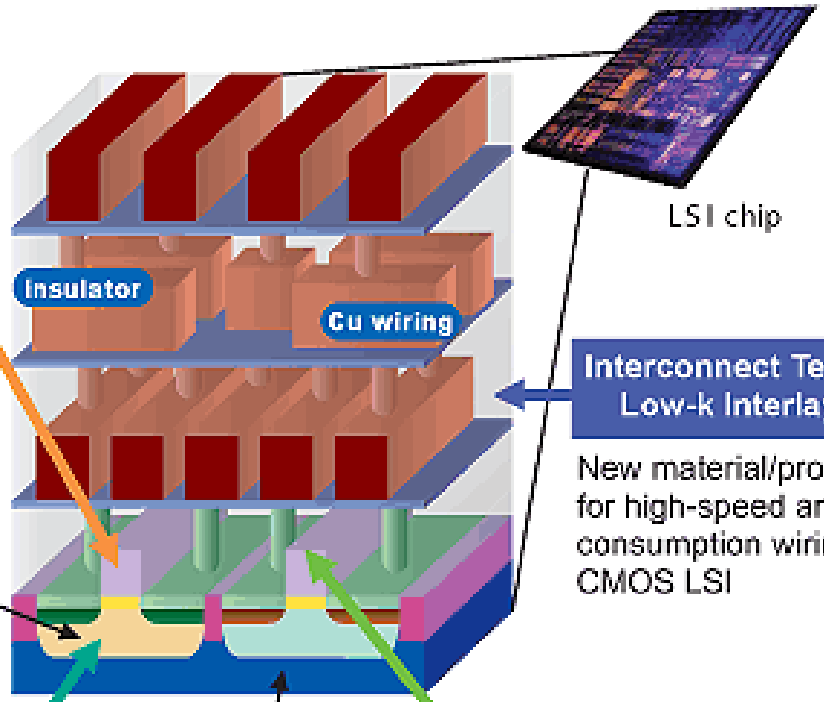
ASET: Semiconductor Process Equipment Technology (Second Stage)

In 1999, ASET made R&D programs for basic technology of next generation semiconductor equipment. They were Advanced Plasma Processing Equipment, Eximer Laser Source, High Speed Processing and Energy Conservation Technology (Self Cleaning Wafer Cassette, High Speed Thermal Processing Technology).

In 2000, R&D of F2 Laser Lithography and Simulation Technology (High Speed High Density Probe Card, High Speed Thermal Processing Technology) programs are continued.

The seven-year MIRAI project (consisting of a three-year first phase and four-year second phase) comprises R&D in new insulating materials, which will be indispensable for semiconductors of the future, and development of the processing technologies necessary for their practical realization. As a result of these activities, the project will develop and demonstrate the feasibility of semiconductor technologies to markedly improve such basic performance features as the power consumption and data processing speed of LSIs in the 45 nm and future technological generations.

IRAI



Gate Stack Technology Using High-k Materials

Development of new materials for gate dielectrics and electrodes, and process/device technology, to realize ultra-small transistors

Interconnect Technology Using Low-k Interlayer Insulators

New material/process technology for high-speed and low-power-consumption wiring in shrunk CMOS LSI

New Transistor Structures and Measurement / Analysis Technology

Development of new device structures and metrology to realize ultimately small, high-performance transistors

Lithography-Related Metrology

Development of metrology and inspection technology for ultra-fine pattern formation

New Circuits and System Technology

Post-fabrication automatic adjustment technology for adaptive correction of waveform distortions and circuit

Selete

Advanced Lithography

- **Optical Lithography and Photomask / Electron Beam Lithography→ 45nm and 65nm nord**

Advanced Process (Front End Process)

- **High-k Material Selection and Film Formation Methods**
- **Ultra Fine Gate Patterning Technology**
- **High-k Wet etching technology**
- **Flash Lamp Anneal Technology**
- **SiN-CVD technology**
- **SiN-Cat-CVD Technology**
- **Base CMOS Module for 65 nm node**
- **High-k transistor module**
- **Metal gated MOSFET Technology**

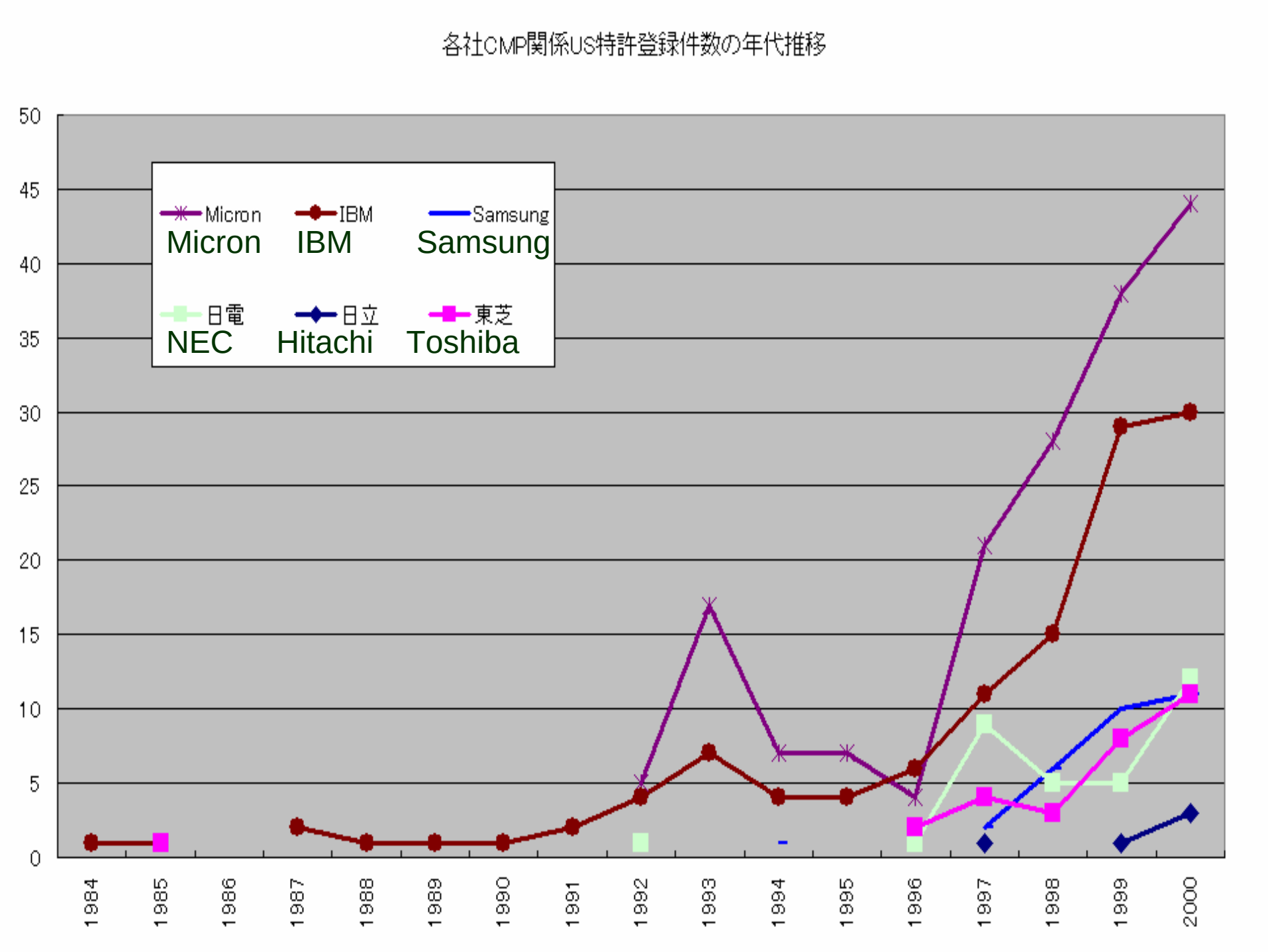
Selete

Advanced Process (Back End Process)

- **Development and evaluation of high-strength porous low-k film**
- **Development of low-damage process**
- **Copper embedding technology using ALD barrier**
- **Evaluation of 200nm pitch, two-level copper interconnect TEG and module fabrication**

Number of accepted papers relating to CMP in IEDM

	89	90	91	92	93	94	95	96	97	98	99	00	01	02	03
Hitachi											★		★		★
Toshiba							★	★		★	★				
NEC					★	★	★	★	★★		★	★			
Mitsubishi															
Fujitsu							★★★				★				★
IBM	★	★		★									★		★
Intel															
Micron					★										
Mostek															
Motorola					★	★	★		★		★				
TI										★					
Infineon +Siemens															
Samsung						★★		★★		★		★	★		★
Hynix +Hyundai + LG															


各社CMP関係US特許登録件数の年代推移
Micron
IBM
Samsung
日電
日立
東芝
NEC
Hitachi
Toshiba
50
45
40
35
30
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5
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1984
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Meaning of CMP and High-k, Low-k

CMP; Eliminating the influence of the difference in under layers and improving independence of following wiring process.

→ Cancellation of process complexity

High-k, Low-k; New material. The material physical properties, the deposition method, and the device structure that are the key factors that decide the process performance depend mutually.

→ Concentrating the knowledge of the device maker, the device manufacturer, and the material manufacturer have to be needed.

CASMAT

Japanese semiconductor materials manufacturers are playing a major role in the world market and will try to continue to offer high quality and advanced semiconductor materials, but are now facing the difficulties to overcome the methodology limit of the individual material research to improve the performance of the comprehensive set materials under the changing circumstances of rapid progress of nano-meter devices and complex processes.

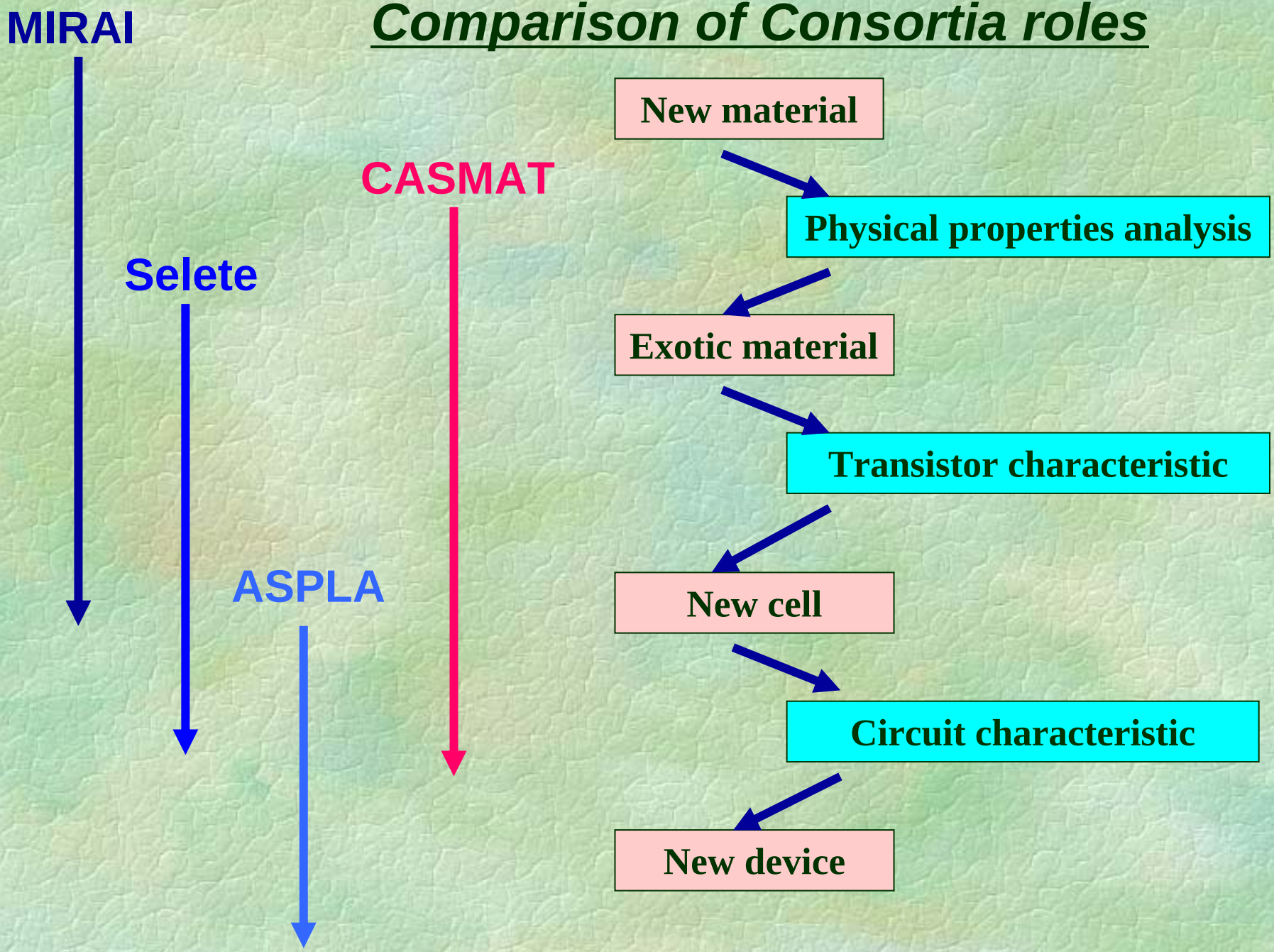
Against this backdrop, **it becomes more and more important to have close cooperation between different manufacturers of semiconductor devices, semiconductor materials and semiconductor equipments in order to promote the concurrent development of processes and materials**, thus achieving the high efficient development of the world's leading new semiconductors and their necessary materials.

Recognizing this importance, Consortium for Advanced Semiconductor Materials and Related Technologies (CASMAT) was formed and founded by a group of major Japanese manufacturers of semiconductor materials in March, 2003

Comparison among MIRAI, Selete, and CASMAT

MIRAI	Selete	CASMAT
65-45nm	65nm ～	65nm
Next generation (65nm), and the exotic material for generation (45nm) and the developments of the process module and the device technology, etc.	1)157 nm lithography, mask, and EPL (electron beam projection exposure lithography)、2) Transistor that adopted an exotic High-k material for gate、3) Multilevel interconnection using an exotic Low-k material and Cu	1) Development of element technology, evaluation technology, and supporting tools for back end process of 65 nm semiconductor devices. 2) Design of TEG(=Test Element Group) for the evaluation of the materials.
・Development of materials, material and measurement and analysis technology for the high-k gate. ・Development of materials, material and measurement and analysis technology for the Low-k insulator. ・Others	Leading edge lithography technology -Optical lithography mask -EB lithography ・Leading edge processing technology（FEP) -High-k Element process -Front end process -Process module ・Leading edge processing technology（BEP) -Back end process	・Material related to the insulation film between low permittivity layers ・Material related to copper interconnect CMP ・Buffer court and material related to re-wiring ・Material related to wafer processing for assembly

Comparison of Consortia roles



Comparison among MIRAI, Selete, and CASMAT

MIRAI	*Selete*	*CASMAT*
Part of AIST (Nationa Institute)	*Company*	*Research Association*
¥3.8 billion in Fiscal 2001, ¥4.56 billion and ¥1.78 billion for extra budget in 2002, ¥4.55 billion in 2003, ¥4.55 billion in 2004, and ¥4.55 billion in 2005. By Advanced Semiconductor Research Center (ASRC) and the Association of Super-Advanced Electronics Technologies (ASET)	Capital: ¥5.5 billion R&D Budget for ASKA project: ¥70 billion / 5years	
ASM Japan; EBARA; Fujitsu; Hitachi Construction Machinery,; Hitachi High-Technologies; Hitachi Kokusai; Intel; Matsushita Electric; Mitsui Chemicals; NEC; Nikon; Oki Electric; Renesas Technology; ROHM; Sanyo; Seiko Epson; Sharp; Sony; Sumitomo Chemical; Sumitomo Heavy Industries; Tokyo Electron; Toshiba, and ULVAC24 companies	Stockholders; Fujitsu; Matsushita Electric; NEC Electronics; Oki Electric; Renesas Technology ; Sanyo ; Seiko Epson ; Sharp ; Sony ; Toshiba Contractors; Samsung	JSR Sumitomo Chemical Sumitomo Bakelite Sekisui Chemical Tokyo Ohka Kogyo Toray Industries Nissan Chemical Nitto Denko Hitachi Chemical Fuji Photo Film Co., Ltd.

Selete engineer A (High-k); Our processes are not leading edge. The development of a top major company is more advanced than we. Therefore the process developed here would not be used in the major semiconductor manufacturer. However, their development doesn't necessarily succeed without fail . If their development fails, the processes of us become the substitutions. On the other hand, the companies in secondary position will use our processes as it is.

Selete engineer B (High-k); The content of our research and the content of the research of MIRAI consequentially become the same almost. Because the device structure depends on the material, and an appropriate material is selected according to the device structure.

☆ Why was the development start to CMP delayed?

→ Japanese semiconductor device manufacturers have the possibility of not noticing the importance of the reduction of the interference between the processes to ease the complexity.

☆ Why were not the device makers, the equipment manufacturers, and the material suppliers able to cooperate for the development of High-k and the Low-k process?

→ Japanese semiconductor device manufacturers did not have adequate management skills for R&D with completely new materials to which physical properties have not been clarified enough. They were not able to get rid of the traditional R&D management progressed gradually based on the improvement of the past.

The increase in the number of processes strongly demanded the improvement of experimental efficiency.

→ STARC ?

The increase in the product development cost strongly demanded the improvement of experimental efficiency.

→ ASPLA ?

The increase in the wafer fabrication cost strongly demanded the improvement of productivity.

→ New joint fab?

Typical examples to cope with rapidly increasing complexity:

- Increasing *ex ante* indeterminacy should be alleviated by *ex post* agility -

- **Software（including embedded system）:**

  Structured programming & Waterfall-style development method

  → Object-oriented programming & UML-based and agile development method（Aspect-oriented method considers even the nonlinearity among objects *per se*）

- **Data base:**

  Era of Relational Database → Era of XML Database

- **CPU architecture:**

  Architecture that aims to secure *ex ante* "high reproducibility" → Architecture that presupposes *ex ante* indeterminacy induced by rapidly increasing complexity（Single-core →Multi-core）

- **Semiconductor device:**

  Design and manufacturing that presupposes the validity of scaling rule

  → Design and manufacturing that presupposes *ex ante* indeterminacy caused by variations in gate length and interconnect geometry

- **Production system:**

  Push-type production system → Pull-type production system（with SCM)

Complexity-Reducing Public Projects in the US：MMST（88－93）

- Microelectronics Manufacturing Science & Technology (MMST) project newly created open object-oriented MES (Manufacturing Execution System)

→Revolutionary execution-based factory management software to easily understand the composition of the whole and part ”.

→Hierarchical visualization at a glance among semiconductor processing technologies

→Texas Instruments as a key player in MMST intended to incorporate Toyota Production System (TPS) in this MES.

→The advent of such a MES with “high visibility” increased the importance of TPS-like organizational management that could enhance employees’ intrinsic motivation.

→The fruits were instantly enjoyed by the US chipmakers through SEMATEC and immediately by the Korean, Taiwanese, and European. (The real dissemination among Japanese ones was the late 90's.)

Summary

- **Against chipmakers' original intention, the governance of most Japanese consortia seems to have cut out even their existing business.**

  → The business that cannot be done in the chip manufacturer cannot be done.

  → Non-participation of material and tool makers

- **To develop state-of-the-art process technologies, several process consortia were consecutively built to follow conventional ways of R&D collaboration.**

  → They could not catch up with the rapidly increasing complexity in process technologies.

- **Since the most of Japanese consortia were built as an allopathy, they could not effectively cope with technologically quite novel complexity.**

  → This might not be limited to Japanese semiconductor consortia.